ULTRA-FAST ADDER

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ABSTRACT

A carry look-ahead adder capable of adding or subtracting
two input signals includes first stage logic having a
10   plurality of carry-create and carry-transmit logic circuits
each coupled to receive one or more bits of each input signal.
Each carry-create circuit generates a novel carry-create
signal in response to corresponding first bit-pairings of the
input signals, and each carry-transmit circuit generates a
15   novel carry-transmit signal in response to corresponding
second bit-pairings of the input signals. The carry-create and
carry-transmit signals are combined in carry look-ahead logic
to generate accumulated carry-create signals, which are then
used to select final sum bits.